International Journal of ChemTech Research
CODEN (USA): IJCRGG ISSN: 0974-4290
Vol.7, No.2, pp 1005-1013, 2014-2015

ICONN 2015 [4th - 6th Feb 2015]
International Conference on Nanoscience and Nanotechnology-2015
SRM University, Chennai, India

Triple Material Gate Work Function Engineering in Surrounding Gate Nanoscale MOSFETs for reduced Short Channel Effects (SCE's): Scale Length Model

G. Lakshmi Priya[1]*, and Dr. N.B. Balamurugan[2]

[1]Thiagarajar College of Engineering, Madurai – 625015, TamilNadu, India

Abstract: In this paper, the concept of Triple Material Gate (TMG) work function engineering is incorporated in the SG Nanoscale MOSFETs, to increase the overall device performance in terms of reduced subthreshold swing and increased immunity against SCE's. A detailed analytical model on scale length determination of Nanoscale SG MOSFETs has been presented based on the solution of 2D-Poisson's equation. The scale length accounts for the effective conduction path of sub-threshold leakage and thereby captures the subthreshold swing. The scale length model can then be used to model the Short Channel Effects (SCEs) in Triple Material Surrounding Gate (TMSG) devices. The scaling factor is also influenced by the depth of the effective conducting path effect d_{eff}.The subthreshold conduction of MOSFET can be described by the Effective Conducting Path Effect (ECPE) and minimum surface potential in that path. The results of our proposed model are compared and verified with other conventional scaling theories. Thus, the proposed scale length model for TMSG Nanoscale devices, shows reduced subthreshold leakage current and enhanced device performance in the sub-nanometer regime.

Keywords: Effective Conducting Path Effect (ECPE), Scaling Theory, Short Channel Effects (SCEs), Subthreshold Conduction, Tri Material Surrounding Gate (TMSG) MOSFET, Two-Dimensional (2-D) modeling.

Introduction

Scaling of device dimensions has been the primary factor, driving improvements in integrated circuit performance and cost which contributes to rapid growth of the semiconductor industry[1-4]. In the nanoscale regime, scaling of transistors has paved the way for reduction of cost and size of devices. Scaling of the natural length gives a measure of the short channel effect inherent to a particular device structure[5-,9]. A two dimensional analysis is necessary to derive scaling theory that properly account for the channel length dependence. Several scaling theories have been developed for various devices [10- 13], but a scaling theory for TMSG MOSFET[14,15,16] is yet to be developed, which is necessary in the era of device scaling, to suppress the short channel effects. In this paper, we propose a new scaling theory for tri material surrounding gate MOSFET with ECPE. The scale length accounts for the effective conduction path of sub-threshold leakage and thereby captures the short channel effects and subthreshold swing [17-20]. With ECPE, our proposed model not only offers a unified scaling rule but also provides a general guideline for tri material surrounding gate MOSFET.

In this paper, we propose a new scaling theory for tri material surrounding gate MOSFET with ECPE. The scale length accounts for the effective conduction path of sub-threshold leakage and thereby captures the short channel effects and subthreshold swing. To derive the scaling theory at subthreshold region, the effective conducting path effect (ECPE) should be accounted for. The scale length model can then be used to model the SCE in TMSG devices and guide for the design to improve their performance. The depth of the effective conducting path d_{eff}provides the location where the punch through current mainly occurs at subthreshold conduction with ECPE mode. In this paper we derive a generalized scaling theory based on the new scaling factor αassociated with ECPE. With ECPE, our proposed model not only offers a unified scaling rule but also provides a general guideline for tri material surrounding gate MOSFET.

Analytical Model for TMSG MOSFETs

Figure.1 shows the schematic structure of the triple material surrounding gate MOSFET. In this structure, the gate electrode consists of three materials M1, M2 and M3 of different work functions deposited over respective lengths L_1, L_2 and L_3 on the gate oxide layers. The gate materials are chosen in such a way that $\phi_{M1} > \phi_{M2} > \phi_{M3}$ and gate length is defined as $L = L_1 + L_2 + L_3$. The gate material at the source end has the highest work function. The middle material has intermediate work function. The material at the drain end is with the lowest work function. This unique feature of TMSG feature is an added advantage when the device dimensions are continuously shrinking. This introduces a step function in the potential along the channel, which in turn reduces Drain induced Barrier Lowering (DIBL) effects and peak electric field at the drain end[7,8,9,10]. The device is composed of gate material 1 with the work function ϕ_{M1}=4.8eV (Au), gate material 2 with ϕ_{M2} =4.6eV (Mo), and gate material 3 with ϕ_{M3} =4.4eV (Ti).

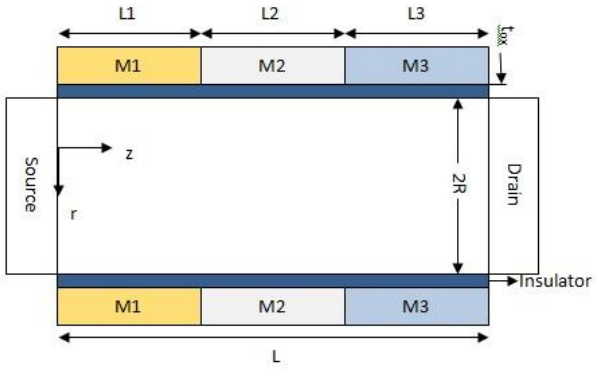

Fig.1. Schematic Cross Sectional View of Fully depleted Triple Material Surrounding Gate (TMSG) SOI MOSFET

The Poisson's equation for potential $\phi(r,z)$ in fully depleted SG MOSFET's is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi(r,z)}{\partial r}\right)+\frac{\partial^2 \phi(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}} \qquad (1)$$

where q is the electronic charge, N_a is the channel doping concentration and ε_{si} is the dielectric constant of silicon. Using the similar manner to Young's[12], we assume that the parabolic potential profile in the vertical direction of the channel is,

$$\phi(r,z) = s_1(z) + s_2(z)r + s_3(z)r^2 \qquad (2)$$

The boundary conditions required for the solution are given as follows[7]

(i) The central position is a function of z only.

$$\phi(0,z) = \phi_c(z) \qquad (3)$$

(ii) The electric field at r = R is given by

$$\frac{\partial \phi(r,z)}{\partial r}\Big|_{r=R} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_s(z) - V_{gs} + V_{fb}}{R\ln\left(1+\frac{t_{ox}}{R}\right)}\right) \quad (4)$$

(iii) The electric field at r=0 is equal to zero.

$$\frac{\partial \phi(r,z)}{\partial r}\Big|_{r=0} = 0 \quad (5)$$

where $V_{fb}$is the flat band voltage, $V_{gs}$is the gate to source voltage and $\phi_s(z)$ is the surface potential along the channel, $2R=t_{si}/2$ is the diameter of the silicon pillar and t_{si} is the thickness of the silicon film, ε_{ox} is the permittivity of the oxide layer, t_{ox} is the gate oxide thickness. The constants in Eq. (2) can be found from boundary conditions (3) to (5),

$$S_2(z) = 0 \quad (6)$$

and

$$S_3(z) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_s(z) - V_{gs} + V_{fb}}{2R^2\ln\left(1+\frac{t_{ox}}{R}\right)}\right). \quad (7)$$

Since $S_1(z), S_2(z)$ and $S_3(z)$ are known, the 2D potential $\phi(r,z)$ in Eq. (2) is expressed as

$$\phi(r,z) = \phi_c(z) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}(2R)}.\frac{V_{gs} - V_{fb} - \phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right] r^2 \quad (8)$$

In Eq. (8), accounting for ECPE, where the most leakage path occurs at $r = d_{eff}$ which is at the position between surface of $r = R$ and channel center of $r = 0$, the potential in the effective conducting path can be obtained as,

$$\phi_{d\,eff}(z) = \phi_c(z) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}(2R)}.\frac{V_{gs} - V_{fb} - \phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right] {d_{eff}}^2 \quad (9)$$

A simple scaling equation is obtained as,

$$\frac{d^2\phi_{d_{eff}}(z)}{dz^2} + \frac{V_{gs} - V_{fb} - \phi_{d_{eff}(z)}}{\frac{1+B-Cd_{eff}^2}{4C}} = \frac{qN_a}{\varepsilon_{si}}\frac{1-A}{1+B-Cd_{eff}^2} \quad (10)$$

where,

$$A = \frac{d_{eff}^2\varepsilon_{ox}}{\varepsilon_{si}(2R^2)\ln\left(1+\frac{t_{ox}}{R}\right)} - \frac{\varepsilon_{ox}}{2*\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (11)$$

$$B = \frac{\varepsilon_{ox}}{2*\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (12)$$

$$C = \frac{\varepsilon_{ox}}{\varepsilon_{si}(2R^2)\ln\left(1+\frac{t_{ox}}{R}\right)} \tag{13}$$

Here we define, $\lambda = \sqrt{\frac{1+B-Cd_{eff}^{2}}{4C}}$ in Eq. (10) as a natural length

$$\lambda = \sqrt{\frac{\varepsilon_{si}Rt_{ox}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}R}{2\varepsilon_{si}t_{ox}}-\frac{\varepsilon_{ox}d_{eff}^{2}}{\varepsilon_{si}(2R)t_{ox}}\right)} \tag{14}$$

In the extreme case of undopedSOI $d_{eff} \approx 0$, the equation Eq. (14) represents the scaling equation proposed by Auth et al. For the high doping case, where $d_{eff} \approx t_{si}/2$, the equation Eq. (14) represents the scaling equation derived by Yan et al. As a consequence, the generalized scaling equation is developed on a base of ECPE and it can be used to develop a generalized scaling factor.

The scaling equation is a second-order 1D differential equation, and can be uniquely solved by specifying two boundary conditions,

$$\phi_{d_{eff}}(z=0) = V_{bi} \tag{15}$$

$$\phi_{d_{eff}}(z=L_{eff}) = V_{bi} + V_{ds} \tag{16}$$

on solving Eq. (10) by using Eq. (15) and Eq. (16) and one obtains

$$\phi_{deff}(z) = \frac{1}{Sinh\left(\frac{L_{eff}}{\lambda}\right)}\left[(V_{bi}+V_{ds}+D)Sinh\left(\frac{L_{eff}-z}{\lambda}\right)+(V_{bi}+D)Sinh\left(\frac{z}{\lambda}\right)\right]-D \tag{17}$$

where

$$D = \frac{qN_a}{\varepsilon_{si}}\frac{1-A}{4C} - V_{gs} + V_{fb} \tag{18}$$

In a conventional surrounding gate MOSFET, the gate is made of only one material, but in the TMSG structure, we have gate made of three different materials with different work functions and doping concentrations under them. On applying Eq. (17) to this device, we have three different potentials under each gate.

$$\phi_{deff1}(z) = \frac{1}{Sinh\left(\frac{L_{eff}}{\lambda}\right)}\left[L \quad Sinh\left(\frac{z}{\lambda}\right)+M \quad Sinh\left(\frac{L_1-z}{\lambda}\right)\right]-D$$

for $0 \le z \le L_1$ (19)

$$\phi_{deff2}(z) = \frac{1}{Sinh\left(\frac{L_{eff}}{\lambda}\right)}\left[L \quad Sinh\left(\frac{z-L_1}{\lambda}\right)+M \quad Sinh\left(\frac{(L_1+L_2)-z}{\lambda}\right)+\right]-D$$

for $L_1 \le z \le L_1+L_2$ (20)

$$\phi_{deff3}(z) = \frac{1}{Sinh\left(\frac{L_{eff}}{\lambda}\right)}\left[L \quad Sinh\left(\frac{z-(L_1+L_2)}{\lambda}\right)+M \quad Sinh\left(\frac{L_{eff}-z}{\lambda}\right)+\right]-D$$

for $L_1+L_2 \le z \le L_1+L_2+L_3$ (21)

The subthreshold conduction can be analyzed by the minimum potential in the effective conducting path. The minimum of the potential will occur at z_{min} by setting,

$$\frac{d\phi_{d_{eff}}(z)}{dz} = 0 \tag{22}$$

substituting Eq. (17) in Eq. (22), we obtain

$$z_{\min} = \frac{1}{2}\lambda \left[\frac{L - M \exp\left(\frac{L_{eff}}{\lambda}\right)}{M \exp\left(-\frac{L_{eff}}{\lambda}\right) - L} \right] \quad (23)$$

where

$$L = V_{bi} + V_{ds} + D \quad (24)$$

$$M = V_{bi} + D \quad (25)$$

By using Eq. (17) and Eq. (23), the minimum potential with ECPE is given by

$$\phi_{d_{eff},\min} \approx \sqrt{LM} \exp\left(\frac{-L_{eff}}{2\lambda}\right) - D \quad (26)$$

andand the minimum channel position is obtained as,

$$z_{\min} \approx \frac{L_{eff}}{2} + \frac{\lambda}{2} \ln\left(\frac{M}{L}\right) \quad (27)$$

The punch-through current at subthreshold region mainly depends on the minimum channel potential of $\phi_{d_{eff},\min}$ induced by the effective conducting path. Hence, the exponential term of Eq. (26) is defined as the scaling factor with ECPE and it is given as,

$$\alpha = \frac{L_{eff}}{2\lambda} \quad (28)$$

Thus the novel scaling factor accounting for ECPE is derived. Once α is determined, the relationship between device parameter of t_{ox} and t_{si} can be expressed by

$$t_{ox} = \frac{\varepsilon_{ox}}{\varepsilon_{si} R} \left[\frac{L^2{}_{eff}}{\alpha^2} + d_{eff}^2 - R^2 \right] \quad (29)$$

Eq. (29) is the key equation to model the device parameters for allowable scaling factor α . Using the above equation we can design the proper device parameter such as t_{ox} and t_{si} to acquire the scaling factor leading to the desired subthreshold swing. By comparing the model proposed by Auth et al., our model is more suitable for SG MOSFET's scaling due to the third term of right-hand side in Eq. (29) which takes various effective conducting paths corresponding to different doping densities into consideration.

Results and Discussions

Figure.2 shows the plot of gate oxide thickness for an effective gate length with different silicon thickness. In addition the calculated gate oxide thickness of double gate MOSFET proposed by Suzuki et al. is included and its results are compared with our tri material surrounding gate MOSFETs. The plot indicates that when L_{eff} is increasingly small, the allowable design space for t_{si} and t_{ox} will become aggressively narrow. Thinnest silicon thickness of t_{si}=20nm is preferred since it gives a good scalability factor with less short channel effect and provides a largest design space for t_{ox} and L. It is also clear that, model proposed by Suzuki underrate the scaling capability in comparison to the proposed model.

Figure.3 shows the variation of minimum L_{eff} with silicon thickness with effective conducting path as a parameter. Thinner oxide thickness and more the d_{eff} value are needed to provide shorter gate length to achieve the stable subthreshold swing of 70mV/dec. To hold a stable subthreshold swing, the thinner oxide of t_{ox}=10nm and an effective conducting path of d_{eff} =0.35t_{si} is preferred. The plot clearly implies that, to effectively reduce the subthreshold swing degradation we need to have thin oxide of t_{ox} with large value of d_{eff}.

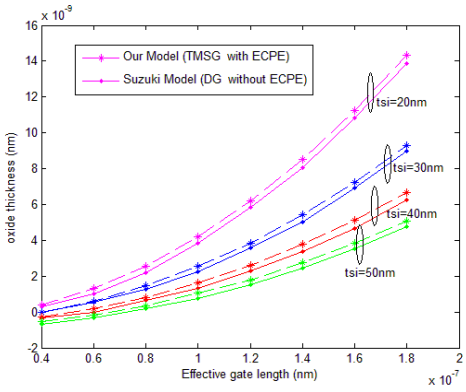

Fig.2.Design contour for double gate MOSFETs and tri material surrounding gate MOSFETs with ECPE for different silicon thickness.

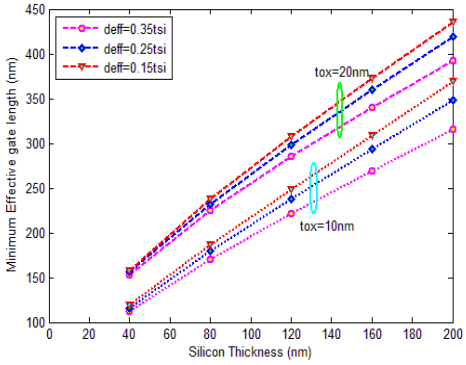

Fig.3.Variation of minimum effective gate length with silicon thickness for different oxide thickness (t_{ox}) and effective conducting paths (d_{eff}).

Figure.4 shows the dependence of subthreshold swing on effective gate length. The subthreshold swing values of tri material surrounding gate MOSFETs with ECPE is compared with the conventional scaling theory results (i.e., without ECPE) proposed by Suzuki et al. and Auth et al. Compared to our model with ECPE, the results predicted by Suzuki et al. underestimate the subthreshold swing because of the unrealistic assumption of surface conduction mode (i.e., $d_{eff} = t_{si}/2$) and the model proposed by Auth et al. overestimates the subthreshold swing because of the assumption of central conduction mode (i.e., $d_{eff} = 0$).

Figure.5 shows the plot of calculated subthreshold swing versus the scaling factor for oxide thickness of t_{ox}=10nm and for silicon thickness of t_{si}=20nm. The figure depicts the subthreshold swing degradation as a function of scaling factor and a scaling factor greater than 4 is required to obtain an ideal subthreshold swing of S=70mV/dec.

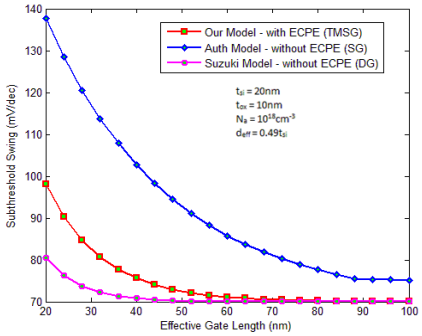

Fig.4. Dependence of subthreshold swing on effective gate length for various analytical models of Auth et.al and Suzuki et.al.

Figure.6 shows the dependence of threshold voltage roll-off on silicon body thickness for various device models. The results of the proposed work are compared with Auth and Suzuki model. Ignoring the effective conducting path effect (ECPE), the results predicted by Auth et al. and Suzuki et al. has a higher threshold voltage roll-off, whereas the calculated results of our proposed model with ECPE shows a lower threshold voltage roll-off. This low threshold voltage roll-off should be taken into consideration in designing the devices.

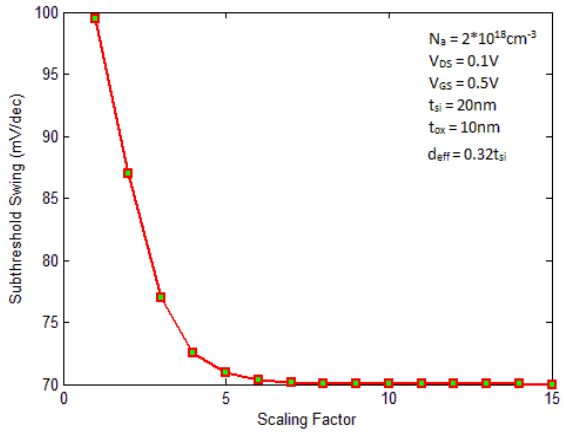

Fig.5. Subthreshold swing versus the scaling factor for oxide thickness of t_{ox}=10nm and for silicon thickness of t_{si}=20nm.

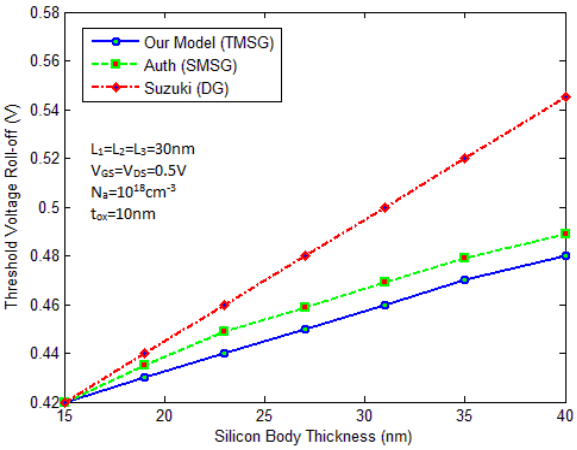

Fig.6. Dependence of threshold voltage roll-off on silicon body thickness for various device models of Auth and Suzuki.

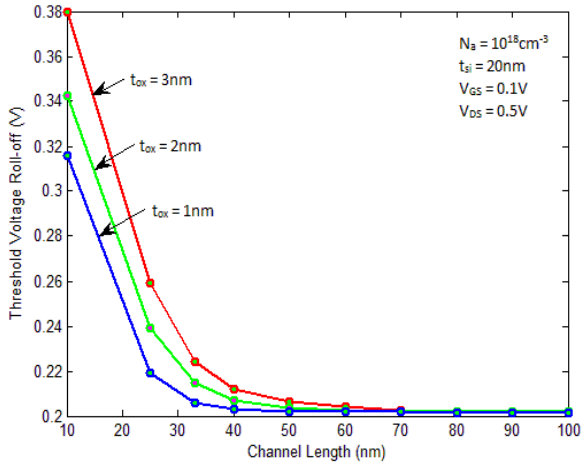

Fig.7. Threshold voltage roll-off with channel length at different gate oxide thickness.

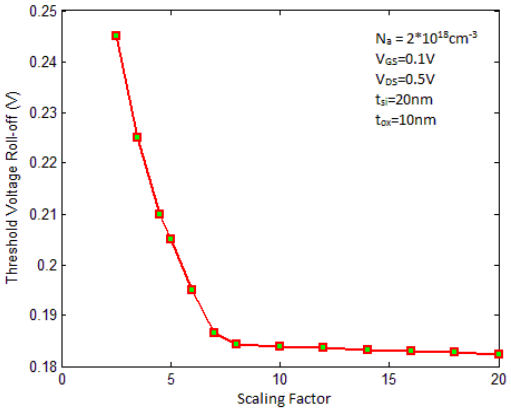

Fig.8. Variation of Threshold voltage roll-off with the scaling factor for TMSG MOSFETs.

Figure.7 shows the threshold voltage roll-off with channel length at different gate oxide thickness. The thin gate oxide of t_{ox}=1nm is superior to thick gate oxide of t_{ox}=3nm in providing small threshold voltage roll-off and it is clearly observed that this thin gate oxide greatly suppresses the short channel effects (SCEs). It is obvious that the thin gate oxide can be used in designing the TMSG for small device technology due to the small threshold voltage roll-off.

Figure.8 shows the influence of scaling factor on threshold voltage roll-off. It is observed that for a large scaling factor the threshold voltage degradation is small. When the scaling factor is beyond 10, the threshold voltage roll-off reduced by drain induced barrier lowering (DIBL) can be avoided.

Conclusions

In this paper, a two-dimensional scaling theory for tri material surrounding gate (TMSG) MOSFETs including effective conducting path effect (ECPE) is presented. The 2D Poisson equation is solved using parabolic approximation approach. The key factor in solving the Poisson's equation with this approach is that it is the best suited method for solving differential equations with boundary values. Effective conducting path effect is taken into account to precisely predict the subthreshold behavior. The natural length and scaling factor is obtained. The small natural length accounts for superb short channel immunity. The device parameters such as oxide thickness and silicon thickness should be properly designed according to the scaling factor to obtain the small natural length and to achieve a stable subthreshold swing. It is also noted that the short channel effects (SCEs) has been reduced greatly with a good scaling factor (in our case $\alpha > 5$). Outweighing the conventional scaling model, this model accounting for ECPE, helps to verify the doping dependent scaling factor which was ignored in the development of the scaling rule in the past. With ECPE, our model provides a good subthreshold swing and a unified scaling rule has been proposed. The proposed work also offers the basic guideline for designing the fully-depleted TMSG MOSFETs. The obtained results are compared with the other conventional scaling theory results to validate this proposed model.

References:

1. Chaudhry and M. J. Kumar, "Controlling short-channel effect in deep-submicron SOI MOSFETs for improved reliability: a review," *IEEETransactions on Electron Devices*, 4, No. 1, 99-109(2006).
2. Endoh T, Mori M ,Sakuraba H and Masuoka F, 'Analysis of short channel effects and proposalof scaling theory in fully depleted double gate SOI MOSFET', *IEICI*, Vol. 2, pp. 72-73 (1999).
3. Fjeldly A and Shur M , 'Threshold Voltage Modeling And sub threshold Regime ofOperation ofShort-Channel MOSFET's', *IEEE Transactions on electron devices*, Vol. 40, No. 1, pp. 137-145 (1993).
4. Frank D J ,Dennard R H,Nowak E , Solomon D.M, Taur Y and Wong H , 'Devicescaling limits of Si MOSFET's and their application dependencies', *Proc. IEEE*, Vol. 89, No. 3, pp. 259-288 (2001).
5. Chiang T K" A new compact sub-threshold behavior model for dual-material surrounding gate(DMSG) MOSFET", *solidstate Electronics*,53,(2009),490-496.
6. Suzuki K and Pindin S, "Short-channel single-gate SOI MOSFET model," *IEEE Trans.Electron Devices*, 50, No. 5,1297–1305(2003).

7. Yan R H, Ourmazd A, and Lee K F, "Scaling the Si MOSFET: from bulk to SOI to bulk,"*IEEETrans. Electron Dev.*, 39, No. 7, 1704-1710 (1992).
8. Suzuki K, Tanaka T, Tosaka Y, Horie H, and Arimoto Y, "Scaling theory for double gateSOI MOSFETs", *IEEE Transactions on ElectronDevices*, 40, No. 12, 2326-2329 (1993).
9. Auth C.P and Plummer J D, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFETs," *IEEE Trans. on Electron Devices*, 18, No. 2, 74-76 (1997).
10. Chiang T K, "A scaling theory for fully-depleted, surrounding-gate MOSFET's: including effective conducting path effect," *Microelectronic Engineering* 77, 175-183(2005).
11. Balamurugan N B, Sankaranarayanan K, and Suguna M, "A new scaling theory for the effective conducting path effect of dual material surrounding gate Nanoscale MOSFETs," *Journal of Semiconductor Technology and Science*, 8,No.1, (2008).
12. Young K K, "Analysis of conduction in fully depleted SOI MOSFETs," *IEEE trans. ElectronDevices*, 36, No. 3,504-506(1989).
13. Chiang T K, "A scaling theory for fully-depleted SOI double-gate MOSFET's: including effective conducting path effect (ECPE)," *Solid-State Electronics 49 (2005) 317*-322.
14. SuveethaDhanaselvam P,Balamurugan N B, "Performance analysis of fully depleted triplematerial surrounding gate (TMSG) SOI MOSFET," *J.Comput Electron (2014) 13:449-455.*
15. SuveethaDhanaselvam P,Balamurugan N B, "Analytical approach of a nanoscale triple material surrounding gate (TMSG) MOSFETs for reduced short-channel effects", *Microelectronics Journal*,44, No.5, 400-404(2013).
16. Nitayami A ,Takato H , Okabe N, SunouchiK.Hieda K ,Horiguchi F , Masuoka F, "Multi-Pillar Surrounding Gate Transistor (M-SGT) for Compact and High-Speed Circuits," *IEEE Trans. Electron Devices* Vol.38, No.3, pp.579-583, 1991.
17. Chiang T K, "A new two-dimensional analytical model for threshold voltage in undoped surrounding-gate MOSFETs," *IEEE Trans. Electron Devices, 2006.*
18. Kaur H ,. Kabra S , Haldar S,Gupta R S., "An Analytical Drain Current Model for Graded Channel Cylindrical/Surrounding Gate MOSFET," *Microelectronics Journal*,Vol.38, no.3, pp.352-359, 2007.
19. J Hsin-Kai Wang, Sean Wu1_, Te-Kuang Chiang2, and Maw-Shung Lee. " A New Two-Dimensional Analytical Threshold Voltage Model for Short-Channel Triple-Material Surrounding-Gate Metal–Oxide–Semiconductor Field-Effect Transistors", *Japanese Journal Of Applied Physics 51* (2012).
20. Tiwari P K,Dubey S,Singh M and Jit S,"A two –dimensional analytical model for thresholdvoltage of short-channel triple-material double-gate metal-oxide-semiconductor filed-effect transistors", *J.Appl.Phys*.108(2010).

*****